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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/689,954	10/21/2003	Jong-Hoon Oh	2003P52608US/I331.109.101	4420

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EXAMINER	
AHMED, HAMDY S	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 11/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/689,954	OH ET AL.	
	Examiner	Art Unit	
	Hamdy S. Ahmed	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 10/21/03 and 4/20/05
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 18, rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 18, is construed as being independent on claim 17 for the following rejection.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1 - 18 are rejected under 35 U.S.C. 102(e) as being anticipated by Yoo, et al. (US No.: 2002/0161968 A1).

As to claim 1, the Yoo reference teaches a random access memory device comprising (see paragraph 17, lines1 - 3): a controller (see paragraph 7, lines 4); a data

bus coupled to the controller (see paragraph 11, line 6) such that data write information is transferred to and from the controller over a data bus (see paragraph 7, lines 1 - 21); multiple memory modules coupled to the data bus and the controller (see paragraph 27, liens 1 – 7), where the system bus includes a number of data buses; (see paragraph 28, lines 1 –2), each memory module having a driver that produces an echo clock signal on an echo pin , the echo clock pin of each memory module being tied to each of the other memory modules and to the controller (see paragraph 17, lines 1 – 3, where the MASTER is the controller), such that during a read operation of the random access memory device the data bus and echo clock have matched loading conditions (see paragraph 11, lines 11 – 20).

As to claim 2, the Yoo reference teaches a method wherein each memory module further includes a buffer (see paragraph 14, lines 1 – 3).

As to claim 3, Yoo reference teaches a method wherein the echo clock pin of each memory module is tied to the buffer of each of the other memory modules (see figure 4).

As to claim 4, Yoo reference teaches a method wherein the buffer is an unused buffer resulting from the memory module using less than its full capacity (in this case the dummy capacitors, i.e. the buffer, see paragraph 33, lines 1 – 7).

As to claim 5, Yoo reference teaches a method wherein the buffer is a dummy buffer added to the memory module. (In this case the dummy capacitors, i.e. the buffer, see paragraph 33, lines 1 – 7).

As to claim 6, Yoo reference teaches a method wherein the random access memory device (see paragraph 16, lines 2 – 3) includes a first and a second memory module

(see paragraph 27, lines 3 – 6) coupled to the data bus (where the system bus includes several data buses, see paragraph 28, lines 1 – 2), the first memory module having a first echo clock driver (in this case, the resistor acts as a driver, see paragraph 27, lines 3 – 12) producing a first echo clock signal and having a first buffer (see paragraph 27, lines 13 - 20), the second memory module having a second echo clock driver producing a second echo clock signal and having a second buffer (in this case, the resistor acts as a driver, see paragraph 27, lines 3 – 12), wherein the first echo clock signal is coupled to the controller (see paragraph 28, lines 1 – 7; any of these signals can act as an echo signal) and to the second buffer and the second echo clock signal is coupled to the controller and to the first buffer such that (see paragraph 28, lines 1 – 7; any of these signals can act as an echo signal because the input is coming from the controller and is connected to the memory module, and then to the data bus; the output goes back to the controller; that constitutes an echo signal.) during a read operation of the random access memory (see paragraph 30, lines 1 – 6) device the data bus and the first and second echo clocks have matched loading conditions (see paragraph 11, lines 15 – 20).

As to claim 7, the Yoo reference teaches a method wherein the random access memory device (see paragraph 17, lines 2 – 3) includes a first, second, third, and fourth memory module (see paragraph 27, line 15) coupled to the data bus (see paragraph 28, lines1 – 5), the first memory module having a first echo clock driver producing a first echo clock signal and having a first buffer (see paragraph 27, lines 13 - 20), the second memory module having a second echo clock driver producing a second echo clock

signal and having a second buffer (see paragraph 28, lines 1 – 7; any of these signals can act as an echo signal), the third memory module having a third echo clock driver producing a third echo clock signal and having a third buffer (in this case, the resistor acts as a driver, see paragraph 27, lines 3 – 12), the fourth memory module having a fourth echo clock driver producing a fourth echo clock signal and having a fourth buffer (in this case, the resistor acts as a driver, see paragraph 27, lines 3 – 12), wherein the first echo clock signal is coupled to the controller (see paragraph 17, lines 1 – 3 where the MASTER is the controller), and to the second, third, and fourth buffers, the second echo clock signal is coupled to the controller and to the first (see paragraph 17, lines 1 – 3, where the MASTER is the controller), third, and fourth buffers, the third echo clock signal is coupled to the controller (see paragraph 17, lines 1 – 3 where the MASTER is the controller), and to the first, second, and fourth buffers (in this case the resistor acts as a driver, see paragraph 27, lines 3 – 12), and the fourth echo clock signal is coupled to the controller (see paragraph 17, lines 1 – 3, where the MASTER is the controller), and to the first, second, and third buffers such that during a read operation of the random access memory device the data bus and the first see paragraph 39, lines 1 – 6), second, third, and fourth echo clocks have matched loading conditions (see paragraph 11, lines 15 – 20).

As to claim 8, the Yoo reference teaches a random access memory device comprising (see paragraph 17, lines 2 – 3): a controller (see paragraph 7, lines 8 – 9); a data bus coupled to the controller (see paragraph 11, line 6) such that data read and data write information is transferred to and from the controller over the data bus (see

paragraph 7, lines 1 - 21); a first memory module coupled to the data bus and to the controller (see paragraph 27, lines 1 – 7), where the system bus includes a number of data buses, (see paragraph 28, lines 1 – 2), the first memory module having a driver that generates an echo clock signal and having a buffer (in this case, the resistor acts as a driver, see paragraph 27, lines 3 – 12); a second memory module coupled to the data bus (see paragraph 28, lines 1 – 5), and to the controller (see paragraph 11, line 6); the second memory module having a driver that generates an echo clock signal (in this case, the resistor acts as a driver, see paragraph 27, lines 3 – 12) and having a buffer (in this case, the resistor acts as a driver, see paragraph 27, lines 3 – 12), the echo clock signal of the second memory module being tied to the buffer of the first memory module and to the controller, the echo clock signal of the first memory module being tied to the buffer of the second memory module and to the controller (see paragraph 11, line 6).

As to claim 9, the Yoo reference teaches a device the buffers of the first and second memory module are off and producing a load, such that during a read operation (see paragraph 12, lines 1 - 5) of the random access memory (see paragraph 17, lines 2 – 3) device the data bus and echo clock of the first memory module have matched loading conditions (see paragraph 11, lines 15 – 20).

As to claim 10, the Yoo reference teaches a device wherein the buffers of the first and second memory module are off and producing a load (see paragraph 11, lines 15 – 20), such that during a read operation (see paragraph 12, lines 1 - 5) of the random access memory (see paragraph 17, lines 2 – 3) device the data bus and the

echo clock of the second memory module have matched loading conditions (see paragraph 11, lines 15 – 20).

As to claim 11, the Yoo reference teaches a method wherein the buffer is an unused buffer from the memory module using less than its full capacity (in this case, the dummy capacitors, i.e. the buffer, see paragraph 33, lines 1 - 7).

As to claim 12, the Yoo reference teaches a method wherein the buffer is a dummy buffer added to the memory module (in this case, the dummy capacitors, i.e. the buffer, see paragraph 33, lines 1 – 7).

As to claim 13, the Yoo reference teaches a method further including a third memory module coupled to the data bus (see paragraph 28, lines 1 – 5), and to the controller (see paragraph 11, line 6), the third memory module having a driver that generates an echo clock signal and having a buffer (in this case, the resistor acts as a driver, see paragraph 27, lines 3 – 12), the echo clock signal of the first memory module being tied to the buffers of the second and third memory modules and to the controller (see paragraph 11, line 6), the echo clock signal of the second memory module being tied to the buffers (in this case the resistor acts as a driver, see paragraph 27, lines 3 – 12), of the first and third memory modules and to the controller, and the echo clock signal of the third memory module being tied to the buffers of the first and second memory modules and to the controller (see paragraph 11, line 6).

As to claim 14, the Yoo reference teaches a system wherein the buffers (in this case the dummy capacitors, i.e. the buffer, see paragraph 33, lines 1 – 7) of the first, second, and third memory modules are off and producing a load, such that during a read

operation of the random access memory device the data bus and each echo clock have matched loading conditions (see paragraph 11, lines 15 – 20).

As to claim 15, the Yoo reference teaches further a device including a fourth memory module (see paragraph 27, line 15) coupled to the data bus (the system bus includes several data buses, see paragraph 28, lines 1 – 2) and to the controller (see paragraph 27 lines 3 – 4), the fourth memory module having a driver (in this case the resister acts as a driver, see paragraph 27 lines3 – 12) that generates an echo clock signal and having a buffer (In this case the dummy capacitors i.e. the buffer see paragraph 33, lines 1 - 7), the echo clock signal of the first memory module (see paragraph 8, lines 9 – 11) being tied to the buffers of the second, third, and fourth memory modules and to the controller, the echo clock signal of the second memory module being tied to the buffers of the first, third, and fourth memory modules and to the controller (see paragraph 8, lines 9 – 11), the echo clock signal of the third memory module being tied to the buffers of the first (in this case, the dummy capacitors, i.e. the buffer, see paragraph 33, lines 1 - 7), second, and fourth memory modules and to the controller (see paragraph 8, lines 9 – 11), and the echo clock signal of the fourth memory module being tied to the buffers of the first, second, and third memory modules and to the controller (see paragraph 8, lines 9 – 11).

As to claim 16, the Yoo reference teaches a method wherein the buffers of the first, second, third, and fourth memory modules (see paragraph 8, lines 9 – 11), are off and producing a load, such that during a read operation (see paragraph 7, lines 14 – 16)

of the random access memory (see paragraph 17, lines 2 – 3) device the data bus and each echo clock have matched loading conditions (see paragraph 11, lines 18 – 20).

As to claim 17, the Yoo reference teaches a random access memory device comprising (see paragraph 17, lines 2 – 3): a controller (see paragraph 11, line 6); a data bus coupled to the controller (see paragraph 11, lines 5 – 8) such that data read and data write information is transferred to and from the controller over the data bus (see par paragraph 15, lines 1 – 26); multiple memory modules coupled to the data bus and to the controller (see paragraph 8, lines 4 – 12), each memory module producing an echo clock signal that is received by the controller (see paragraph 18, lines 1 – 4, where the MASTER is the controller) during a read operation (see paragraph 15, line 20) of the random access memory device (see paragraph 17, lines 2 – 3) and each memory module including means for matching the loading conditions of the data bus and the memory modules (see paragraph 11, lines 18 – 20).

As to claim 18, the Yoo reference teaches a method wherein each memory module has a driver that produces an echo clock signal (in this case, the resistor acts as a driver, see paragraph 27, lines 3 – 12), the echo clock signal of each memory module being received by each of the other memory modules and by the controller (see paragraph 13, lines 1 – 20; each of these signals is an echo signal), such that during a read operation (see paragraph 15, line 20) of the random access memory (see paragraph 17, lines 2 – 3) device the data bus (see paragraph 11, line 6) and echo clock have matched loading conditions (see paragraph 11, lines 15 – 20).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hamdy S. Ahmed whose telephone number is 571-270-1027. The examiner can normally be reached on M-TR 7:30-5:00pm and Every 2nd Friday 7:30-4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hung Sough can be reached on 571-272-4199. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

HA

Hamdy Ahmed

11/22/06

HYUNG SOUGH

SUPERVISORY PATENT EXAMINER

11/21/06